AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-20. Cancelled.

21 (new). A wafer prober for probing a semiconductor wafer having a ceramic substrate and a conductor layer formed on a surface of said ceramic substrate, wherein said ceramic substrate comprises at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

22 (new). The wafer prober according to Claim 21, wherein said ceramic substrate is equipped with a temperature control means.

23 (new). The wafer prober according to Claim 22, wherein said temperature control means is a heating element.

24 (new). The wafer prober according to Claim 21, wherein said ceramic substrate is equipped with a Peltier device.

25 (new). The wafer prober according to claim 21, wherein channels are formed on said surface of said ceramic substrate.

26 (new). The wafer prober according to Claim 25, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

27 (new). The wafer prober according to Claim 21, wherein said conductor layer is a chuck top conductor layer.

28 (new). The wafer prober according to Claim 21, wherein said conductor layer has a thickness of 1 to 20 μm.

29 (new). The wafer prober according to Claim, 21, wherein a noble metal layer is formed on said surface of said conductor layer.

30 (new). The wafer prober according to Claim 21, wherein said conductor layer comprises nickel.

31 (new). The wafer prober according to Claim 21, wherein said conductor layer comprises a titanium layer, a molybdenum layer and a nickel layer in this order.

32 (new). The wafer prober according to Claim 21, which performs a probing of a semiconductor wafer by pressing a probe card on the wafer.

33 (new). A wafer prober for probing a semiconductor wafer having a ceramic substrate and a conductor layer formed on a surface of said ceramic substrate and at least one conductor layer formed inside said ceramic substrate.

34 (new). The wafer prober according to Claim 33, wherein said ceramic substrate is equipped with a temperature control means.

35 (new). The wafer prober according to Claim 34, wherein said temperature control means is a heating element.

36 (new). The wafer prober according to Claim 21, wherein said conductor layer comprises porous material.

37 (new). The wafer prober according to Claim 36, wherein said conductor layer has a thickness of 1 to 200 μm.

38 (new). The wafer prober according to Claim 36, wherein said conductor layer is a chuck top conductor layer.

39 (new). The wafer prober according to Claim 36, wherein said ceramic substrate is equipped with a temperature control means.

40 (new). The wafer prober according to Claim 36, wherein said ceramic substrate is equipped with a Peltier device.

41 (new). The wafer prober according to claim 39, wherein said temperature control means is a heating element.

42 (new). The wafer prober according to Claim 36, wherein at least one conductor layer is formed inside said ceramic substrate.

43 (new). The wafer prober according to Claim 36, wherein channels are formed on said surface of said ceramic substrate.

44 (new). The wafer prober according to Claim 43, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

45 (new). The wafer prober according to Claim 36, wherein a noble metal layer is formed on the surface of said conductor layer.

46 (new). The wafer prober according to Claim 36, wherein said conductor layer comprises nickel.

47 (new). The wafer prober according to Claim 36, wherein said conductor layer comprises a titanium layer, a molybdenum layer and a nickel layer in this order.

48 (new). A ceramic substrate for a wafer prober which has a conductor layer formed on a surface thereof, wherein said ceramic substrate is composed of at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

49 (new). The ceramic substrate for a wafer prober according to Claim 48, wherein said ceramic substrate is equipped with a temperature control means.

50 (new). The ceramic substrate for a wafer prober according to Claim 49, wherein said temperature control means is a heating element.

51 (new). The ceramic substrate for a wafer prober according to Claim 48, wherein said ceramic substrate is equipped with a Peltier device.

52 (new). The ceramic substrate for a wafer prober according to Claim 48, wherein channels are formed on said surface of said ceramic substrate.

53 (new). The ceramic substrate for a wafer prober according to Claim 52, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

54 (new). The ceramic substrate for a wafer prober according to Claim 48, wherein said conductor layer is composed of porous material.

55 (new). A ceramic substrate for a wafer prober which has a conductor layer formed on a surface thereof and at least one conductor layer formed inside said ceramic substrate.

56 (new). The ceramic substrate for a wafer prober according to Claim 55, wherein said ceramic substrate is equipped with a temperature control means.

57 (new). The ceramic substrate for a wafer prober according to Claim 56, wherein said temperature control means is a heating element.

AMENDMENTS TO THE DRAWINGS

Please replace Figures 9 and 10 and 11 with the drawings on the attached replacement sheets. The attached replacement sheets of drawings includes changes to Figures 9 and 10 and 11 and replaces the original drawing sheets including the Figures 9 and 10 and 11.

Attachment: Replacement Sheets